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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/046,979	01/17/2002	Yoshiaki Toyota	ASA-1050	5404

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MATTINGLY, STANGER & MALUR, P.C.
Suite 370
1800 Diagonal Road
Alexandria, VA 22314

EXAMINER	
DUONG, THOI V	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/046,979	TOYOTA ET AL.	
	Examiner	Art Unit	
	Thoi V Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 27 February 2004.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 11-13 and 16 is/are allowed.

6)☒ Claim(s) 1-10,14 and 15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 27, 2004 has been entered.

Accordingly, claims 1 and 11 were amended and new claim 16 is added. Currently, claims 1-16 are pending in this application.

Response to Arguments

2. Applicant's arguments with respect to claims 1-10, 14 and 15 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 10, 14 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Zhang (USPN 5,814,529).

Re claim 1, as shown in Figs. 1A-1E, Zhang discloses an image display having a plurality of thin film transistors and a plurality of capacitors on a substrate 101, wherein

a plurality of gate-lines 105 and a plurality of signal-lines 118 which cross said plurality of gate-lines in a matrix shape are formed on said substrate,

each of said thin film transistors has: an island-shaped semiconductor layer 103 having a source region, a drain region, and a channel region sandwiched between them (Fig. 1A); a first insulation film 104 formed between said island-shaped semiconductor layer and a gate electrode 106 of the same layer as that of said gate-lines; an interlayer insulation film 109 formed above said island-shaped semiconductor layer; and a source electrode 116 and a drain electrode 117 which are come into contact with said source region and said drain region via an opening formed in said interlayer insulation film and which exist in the same layer as that of the signal-lines (Figs. 1C-1E), and

each of said capacitors 119 has: a storage electrode 107 of the same layer as that of said gate-lines 105; a second insulation film 108 formed on said storage electrode so as to be in contact therewith (Fig. 1B); and an electrode 115 which is formed on said second insulation film so as to be in contact therewith via an opening 112 formed in said interlayer insulation film and which exists in the same layer as that of said signal-lines,

said first insulation film 104 being formed so as to cover said substrate 101 (Fig. 1A), and said second insulation film 108 being formed so as to be in contact with an upper surface and side surfaces of said storage electrode 107 and an upper surface of said first insulation film 104.

Re claim 2, Zhang also discloses that by setting a suitable etching condition, a silicon nitride film can be used for the second insulating film as an etching stopper (col.

3, lines 34-40). It is inherent that the relative permittivity of said second insulation film is higher than that of said first insulation film which is made of silicon oxide (col. 3, lines 15-18).

Re claim 4, said second insulation layer 108 is formed in an upper portion and a side portion of said gate electrode 106 (Fig. 1B).

Re claim 10, said island-shaped semiconductor layer is an island-shaped polysilicon layer (col. 3, lines 12-28).

Re claims 1, 3, 14 and 15, as shown in Figs. 2A-2E, Zhang discloses a manufacturing method of an image display (as well as the image display device), comprising the steps of:

forming a plurality of island-shaped semiconductor layers 203 onto a substrate 201;

forming a first insulation film 204 onto said island-shaped semiconductor layers;

forming a gate electrode 206 and a storage electrode 207 onto said first insulation film;

forming a source region, a drain region, and a channel region sandwiched between them onto said island-shaped semiconductor layers 203;

forming a second insulation film (oxide film of the storage electrode 207) onto said storage electrode (Fig. 2A);

forming interlayer insulation films 209 onto regions above said gate electrode and said storage electrode;

patterning said second insulation film (oxide layer), and etching only said second insulation film except for an upper surface and side surfaces of said storage electrode 207 and an upper surface of said first insulation film 204 (col. 4, lines 18-32);

forming interlayer insulation film 209 onto regions above said gate electrode and said storage electrode;

simultaneously removing said interlayer insulation film 209 of a contact hole portion 212 and said interlayer insulation film above said storage electrode (Fig. 2B); and

simultaneously forming an electrode 213 on said second insulation film and a source electrode 216 and a drain electrode 217 which are connected to said source region and said drain region,

wherein said second insulation film is formed to an upper portion and a side portion of said gate electrode simultaneously with said step of forming the second insulation film onto said storage electrode (col. 4, lines 22-32).

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (USPN 5,814,529) in view of Tanabe et al. (USPN 5998838).

The image display of Zhang includes all that is recited in claim 6 except that the first insulation film is not a laminate film of a silicon oxide film and a high dielectric constant film. As shown in Fig. 1(b), Tanabe discloses a thin film transistor comprising a gate insulating layer which is a laminate film of a first layer 5 formed of silicon dioxide and a second layer 6 formed of silicon nitride which is higher permittivity than silicon dioxide so as to improve the electrical properties of the interface between the

semiconductor layer and the adjacent gate insulating layer as well as to gain a desired MOS capacitance without thinning the gate insulating layer down to a minimum (col. 9, lines 1-9). Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the display of Zhang with the teaching of Tanabe et al. by forming the first insulation film as a laminate film of a silicon oxide film and a high dielectric constant film so as to improve the electrical properties of the interface between the semiconductor layer and the adjacent gate insulating layer and to reduce the threshold value in operating the thin film transistor.

6. Claims 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (USPN 5,814,529) in view of Jung et al. (USPN 6,317,173 B1).

The image display of Zhang includes all that is recited in claims 5 and 7 except for a parallel capacitor and relative permittivity of the insulation films. As shown in Figs. 19 and 20, Jung discloses a liquid crystal display comprising a parallel capacitor including:

a first capacitor constructed by a polycrystalline silicon layer 200, a first insulation film 300, and a storage electrode 420; and

a second capacitor constructed by said storage electrode, a second insulation film 500 and an interlayer insulation film 700 which is formed on said storage electrode, and a pixel electrode 800 (col. 3, lines 48-59), wherein the first insulating layer 300 may be made of SiO2 or SiNx and the second insulating layer may be made of SiO2 or SiNx (col. 6, lines 35-39 and 57-59) for obtaining a sufficient storage capacitance for the display (col. 24, lines 30-34).

As known in the art, the relative permittivity of SiNx (=7) is higher than that of SiO2 (=4). Accordingly, if the second insulation film is made of SiNx and the first insulation film is made of SiO2, the relative permittivity of the second insulation film is higher than that of the first insulation film. Also, the first insulation film and the second insulation film can be made of a same high dielectric constant material (SiNx).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the LCD device of Zhang with the teaching of Jung by forming an additional capacitor constructed by a polycrystalline silicon layer, a first insulation film, and a storage electrode so as to obtain a sufficient storage capacitance for the display (col. 31, lines 1-13).

7. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (USPN 5,814,529) in view of Hara et al. (USPN 6,046,790).

The image display of Zhang includes all that is recited in claims 8 and 9 except for a frame memory. As shown in Figs. 10-12, Hara discloses a LCD device comprising a frame memory 35 provided in a pixel and constructed by a capacitor 3 and a switch 5 formed on a substrate in order to temporarily store image data (col. 30, lines 5-9) so as to obtain a fast response speed for the display (col. 31, lines 1-13). Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the image display of Zhang with the teaching of Hara by forming a frame memory constructed by a capacitor and a switch so as to obtain a fast response speed for the display (col. 31, lines 1-13).

Allowable Subject Matter

8. Claims 11-13 and 16 are allowed.

The following is an examiner's statement of reasons for allowance: none of the prior art of record fairly suggests or shows all of the limitations as claimed. Specifically,

Re claim 11, none of the prior art of record discloses, in combination with other limitations as claimed, a second insulation film formed in contact with a storage electrode, an upper surface of an interlayer insulation film, and a side surface of the opening formed in said interlayer insulation film.

The most relevant reference, USPN 5,814,529 of Zhang and USPN 6,493,046 B1 of Ueda, fail to disclose or suggest a storage capacitor comprising a second insulation film formed in contact with the storage electrode, an upper surface of the interlayer insulation film, and a side surface of the opening formed in said interlayer insulation film. The Zhang's reference only discloses a second insulation film 108 formed in contact with the storage electrode 107 as shown in Figs. 1A-1E. Meanwhile, as shown in Fig. 1, the Ueda's reference discloses a storage capacitor comprising a storage electrode 17a formed at the same layer as that of semiconductor layer 17, a dielectric layer 18a formed in contact with the storage electrode 17a, and an storage counter electrode 19a formed on the dielectric layer; however, the structure of this storage capacitor is different from that of the present invention in which the storage electrode is formed at the same layer as that of the gate-lines and the storage electrode is formed at the same layer as that of signal-lines.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (571) 272-2293.

Thoi Duong

05/06/2004

ROBERT H. KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800